

*Atty Docket: IDF 1502 (4000-02800)**Patent***REMARKS/ARGUMENTS*****Status of claims***

At the time of the office action of August 24, 2004, claims 1-19 were pending in the present application. Claims 1-19 were rejected on various grounds.

By the present amendment, claims 1-19 have been cancelled and new claims 20 -25 have been presented. Reconsideration of claims 20-25 is respectfully requested.

***Specification***

The abstract was objected to. By the present amendment, a new abstract is submitted and is believed to conform to the requirements for an abstract.

Two paragraphs have also been amended to provide current identification information for two prior patent applications that were incorporated by reference into the present application.

***Drawings***

The Examiner required that Figs. 1-3 be labeled as prior art. Submitted with this amendment is a replacement sheet for Figs. 1-3 in which each figure has been labeled as prior art.

***New claims***

Claims 20-25 are directed to the preferred embodiment of the invention. The preferred embodiment is illustrated in Fig. 6 and is described in detail on pages 15-20 of the present specification.

The background section of the application describes several prior art arrangements for clock synchronization in telecommunications systems that couple analog signals across digital networks. In Fig. 1, the PSTN is a digital system that couples communication signals between telephone company central offices, COs. The PSTN includes its own embedded clock signal that

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is coupled to the COs and is used directly so that no synthetic synchronization is needed. In Fig. 2 a typical ATM network does not have an embedded clock, but highly accurate clocks may be provided in the central offices to ensure synchronization. However, the present invention is directed to integrated services hubs used in residential or business telecommunication systems where the cost, space requirements and power consumption of such clocks is prohibitive. In Fig. 3, a phase locked loop may be used to recover a clock signal based on the arrival rate of digitized packets or samples at a receiving end of the network. While phase locked loops are known circuits, they are typically separate circuits and are not desirable in residential or business telecommunication systems due to the cost, space and increased power consumption and heat dissipation that would result from use of such additional circuitry.

As described in the specification, and the patents incorporated by reference therein, it is highly desirable in residential or business telecommunication systems to minimize the cost, size, and power dissipation of such systems. One way that this is done is the use of the CPU 50 to control and operate as many integrated services hub functions as possible. Not only does this reduce the number of physical circuit chips, but it allows great flexibility since the functions are implemented in software.

New claims 20-25 are directed to the preferred embodiment, Fig. 6, in which the synchronized sample rate is recovered from incoming digital samples by use of the CPU 50 that controls most other functions in the integrated services hub. The system uses an internal clock that is required for the CPU anyway (see page 17, lines 1-2). The input buffer is implemented in memory that is required for a CPU and is controlled by the CPU to act as an input signal buffer for coupling signals to the CODEC (see page 16, lines 4-9). Since the CPU implements and controls the input buffer, the CPU easily provides an indication of fill level of the buffer (see

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page 18, lines 5-11). The CPU includes baud rate generators (see page 17, lines 20-21) that receive the existing internal clock and provide an output sampling signal based on a divisor. In this case, the CPU generates the divisor based on the fill level of the buffer that it controls (see page 18, line 21 through page 19, line 3). Thus the synthetic sampling rate recovery is generated within the CPU.

The references cited by the Examiner do not teach or suggest the recovery of the sampling rate as now claimed and do not teach or suggest the claimed system and method in a residential or business telecommunications system. As a result of these substantial differences, the Applicants submit that claims 20-25 are allowable over the cited references.

*Atty Docket: IDF 1502 (4000-02800)**Patent***CONCLUSION**

Applicants respectfully submit that the present application as amended is in condition for allowance. If the Examiner has any questions or comments or otherwise feels it would be helpful in expediting the application, he is encouraged to telephone the undersigned at (972) 731-2288.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 21-0765, Sprint.

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Respectfully submitted,

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